AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently amended) A packet buffer control system comprising:

a memory storing bytes of data in lines;

a packet buffer, the packet buffer divided into a first section and a second section, each section for storing bytes of data in lines; and

a packet buffer controller that receives a line of data from said memory along with a tag indicating a shift value and shifting said received line of data in accordance with the shift value for storage in said first section and in said second section, wherein storage in said first section and in said second section occur simultaneously.

2. (Original) The packet buffer control system of claim 1 wherein said packet buffer controller comprises a wrap-around shift register in which said received line of data is shifted for storage.

3. (Original) The packet buffer control system of claim 1 further comprising means for masking a line in said packet buffer.

4. (Original) The packet buffer control system of claim 1 wherein storage of a line of data in the first section and in the second section is accomplished in a single clock cycle.

5. (Original) The packet buffer control system of claim 1 wherein the packet buffer controller further includes logic that reads a first output data line from the first section and then reads a second output data line from the second section for transmission to a network.

6. (Currently amended) A method of communicating alignment information comprising:

preparing read requests for lines of data to fill a packet payload;

obtaining a shift value corresponding to any misalignment between the lines of data and the packet payload;

sending a read request including a tag with the shift value, said tag being for inclusion in a response to the read request;

receiving at a packet buffer controller the response having a line of data and the tag; and

shifting the line of data in accordance with the shift value in the tag and writing the shifted line of data into a first section and a second section of the packet buffer, wherein writing the shifted line of data into said first section and said second section occur simultaneously.

7. (Original) The method of claim 6 wherein writing the shifted line of data is accomplished in a single clock cycle.

8. (Original) The method of claim 6 wherein said act of writing writes bytes of the shifted line of data that are in unmasked positions of the packet buffer into the packet buffer while bytes of the shifted line of data in masked positions of the packet buffer do not make changes to the masked positions of the packet buffer.

9. (Original) The method of claim 6 further including:

reading a first output data line from said first section and then reading a second output data line from said second section for transmission to a network.